IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
CASSAGNES

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **CIRCUIT FOR THE DECODING OF BIPHASE SIGNALS**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL 768137862 US
DATE OF DEPOSIT: December 31, 2001
NAME: Dawn Kimler
SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label certain elements in FIGS. 2-4 and 6 in accordance with the specification. No new matter is being added.

In the Claims:

Please cancel Claims 1 to 12.

Please add new Claims 13 to 35.

13. A decoding circuit for decoding a biphase signal having a pair of states and comprising:

a precharging register for precharging the states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit for comparing the two states of the pair of states to detect an error and providing an error signal based upon detecting the error.

14. The decoding circuit of Claim 13 wherein the error comprises the two states being equal.

15. The decoding circuit of Claim 13 wherein the pair of states represent a value, and wherein said verification circuit also provides a decoded signal indicating the value of the precharged pair of states.

16. The decoding circuit of Claim 15 further comprising a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

17. The decoding circuit of Claim 13 further comprising a delay circuit connected to said verification circuit and providing an end signal indicating an end of the biphase signal after a predetermined delay, said delay circuit being initialized at the beginning of the biphase signal.

18. The decoding circuit of Claim 13 further comprising a filter upstream from said precharging register for filtering the biphase signal.

19. A decoding circuit for decoding a biphase signal having a pair of states representing a value, the decoding circuit comprising:

a precharging register for precharging the states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit for comparing the two states of the pair of states and providing an error signal if the two states are equal, said verification circuit also providing a decoded signal indicating the value of the precharged pair of states.

20. The decoding circuit of Claim 19 further comprising a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

21. The decoding circuit of Claim 19 further comprising a delay circuit connected to said verification circuit and providing an end signal indicating an end of the biphase signal after a predetermined delay, said delay circuit being initialized at the beginning of the biphase signal.

22. The decoding circuit of Claim 19 further comprising a filter upstream from said precharging register for filtering the biphase signal.

23. A circuit for transmitting and receiving biphase signals having respective pairs of states and comprising:

transmission and reception circuitry for sending and receiving the biphase signals; and

a decoding circuit coupled to said reception circuitry for decoding the biphase signals and comprising

a precharging register for precharging respective states of the biphase signals, one state of each pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit for comparing the two states of each pair of states to detect an error and providing an error signal based upon detecting the error.

24. The circuit of Claim 23 wherein the biphase signals are encoded according to the digital addressable lighting interface (DALI) communications protocol.

25. The circuit of Claim 23 wherein the error comprises the two states being equal.

26. The circuit of Claim 23 wherein the pair of states represent a value, and wherein said verification circuit also provides a decoded signal indicating the value of each precharged pair of states.

27. The circuit of Claim 26 wherein said decoding circuit further comprises a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

28. The circuit of Claim 23 wherein said decoding circuit further comprises a delay circuit connected to said verification circuit and providing an end signal indicating an end of each biphase signal after a predetermined delay, said

delay circuit being initialized at the beginning of each biphase signal.

29. The circuit of Claim 23 wherein said decoding circuit further comprises a filter upstream from said precharging register for filtering the biphase signals.

30. A method for decoding a biphase signal having a pair of states, the method comprising:

precharging one of the pair of states of the biphase signal into a precharging register at each pulse of a periodic precharging signal;

comparing the two states of the precharged pair of states to detect an error; and

providing an error signal based upon detecting the error.

31. The method of Claim 30 wherein the error comprises the two states being equal.

32. The method of Claim 30 further comprising supplying a decoded signal indicating a value of the precharged pair of states.

33. The method of Claim 32 further comprising storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

34. The method of Claim 30 further comprising measuring a predetermined time from a start of the biphase signal, and providing an end signal after the predetermined

time indicating an end of the biphase signal.

35. The method of Claim 30 further comprising filtering the biphase signal prior to precharging each of the pair of states.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner=s convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

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Filed: **Herewith**

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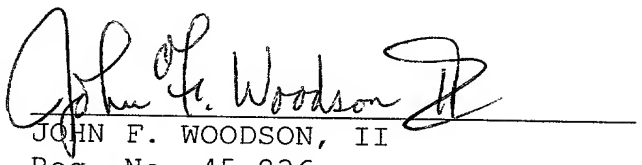
Respectfully submitted,



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SUBMISSION OF PROPOSED DRAWING MODIFICATIONS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label certain elements in FIGS. 2-4 and 6 in accordance with the specification. No new matter is being added.

Respectfully submitted,

John F. Woodson II

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FIG_1 (PRIOR ART)

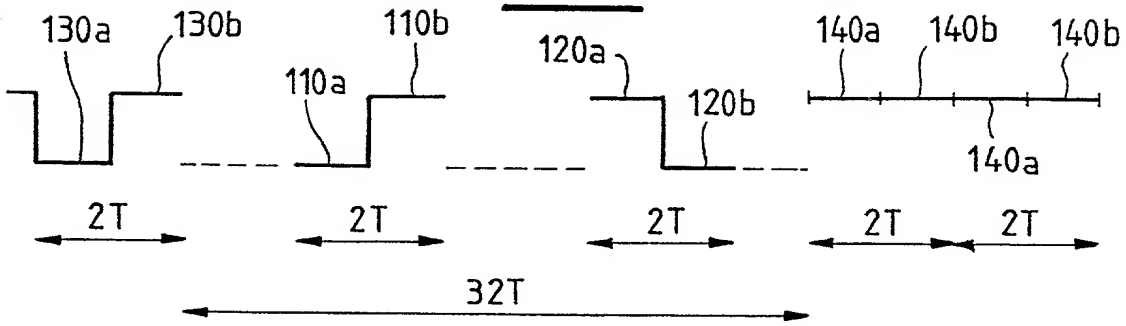


FIG_2

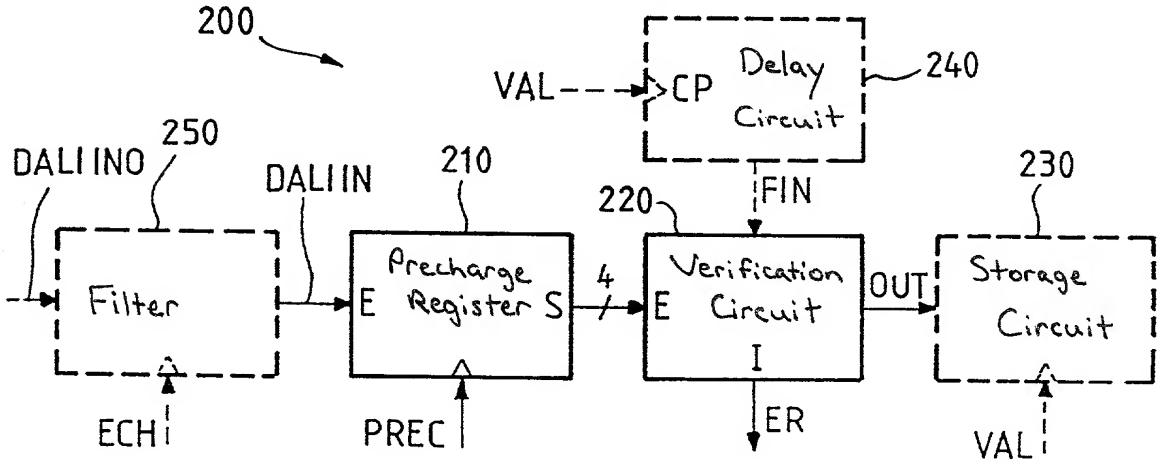


FIG_3

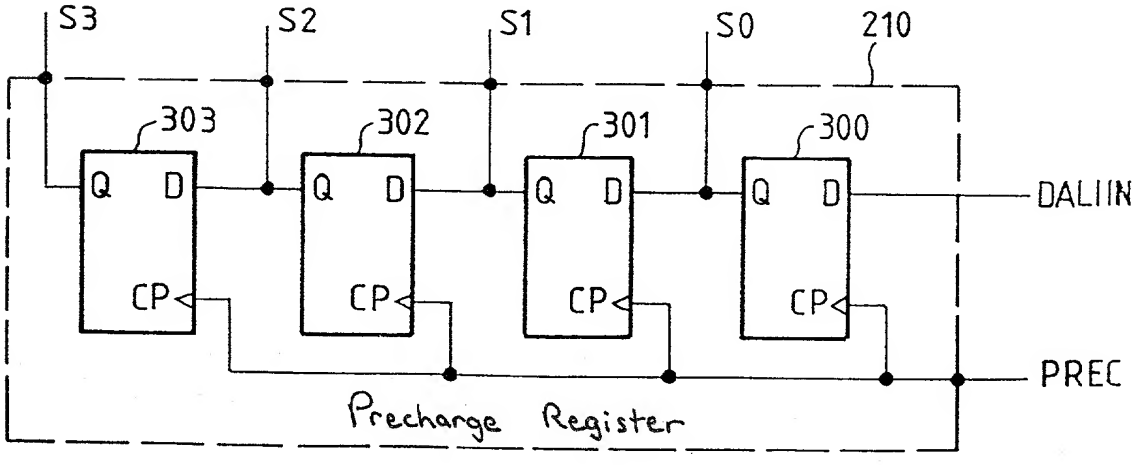


FIG_4

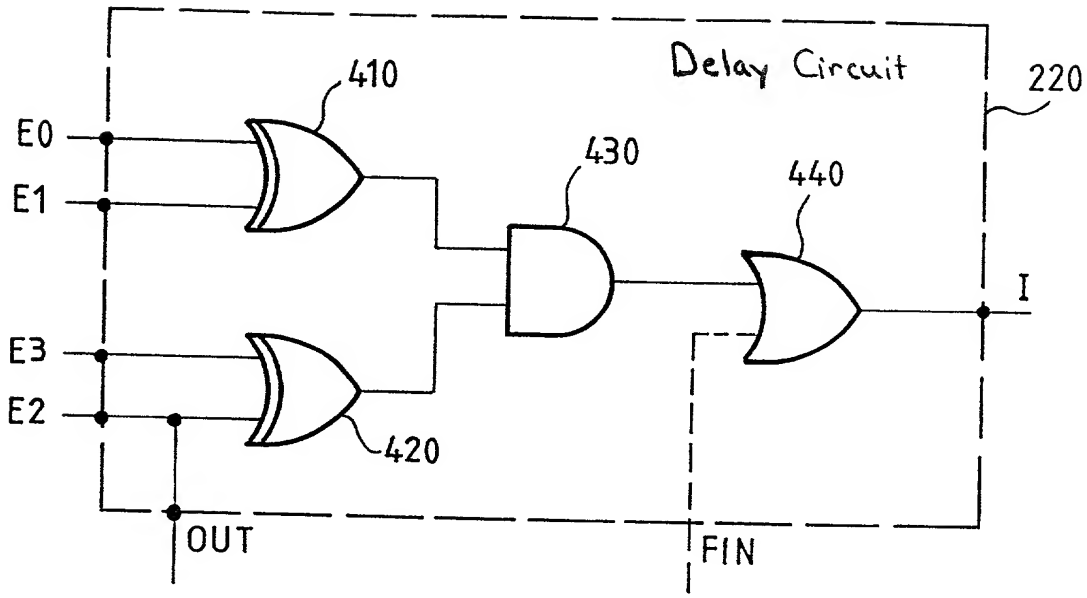
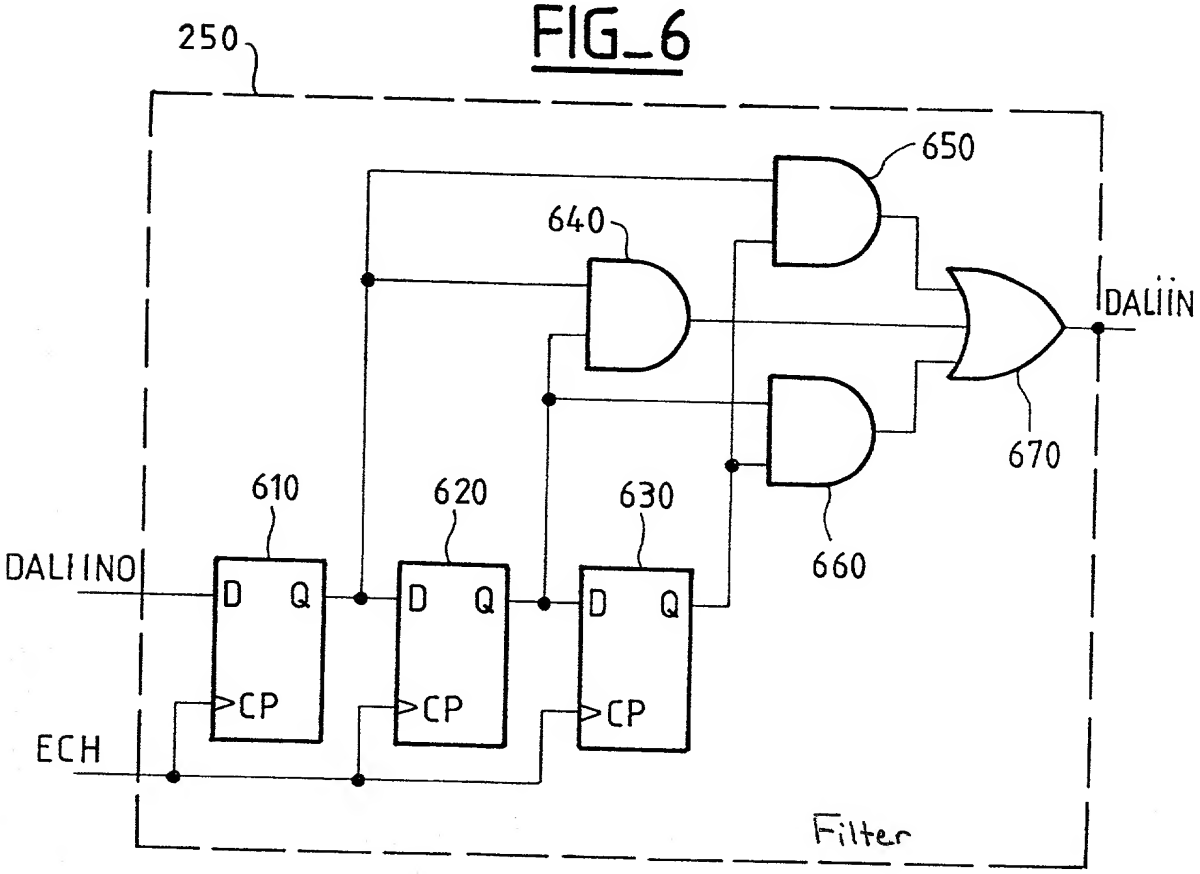

Delay Circuit
220
410
430
440
E0
E1
E3
E2
420
I
OUT
FIN

FIG_6


250
650
640
DALIIN
670
610
620
630
660
DALIINO
D Q
CP
ECH
Filter